

Design Sleep Mode and Wakeup Method for OpenFlow Switches

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Abstract- In this paper, we present a design and an evaluation of two power management modes that reduce the energy consumption of OpenFlow switches. First, we define two new low power modes: SLEEP PORT and SLEEP SWITCH, which reduce energy consumption in cases where packets on port or switches are absent. Second, we present a Wake on LAN (WOL) method for OpenFlow Switches to wake up Ethernet ports or the whole switch from inactive states. Finally, we describe our design, experimental results and performance evaluations. Our results show that the control *SLEEP PORT* mode on a switch might save about 9.8% power consumption per port, and up to about 60% of total power consumption of the switch with *SLEEP SWITCH* mode. In addition, we will implement this method to Openflow Switch bases on NetFPGA- 10 Gigabit in the future.

Keywords- *OpenFlow Switch; NetFPGA; Low Power; Data Center Network; Green Networking.*

I. INTRODUCTION

Power consumption in the ICT infrastructure is a pressing concern. Electricity used by data centers worldwide increased about 56% from 2005 to 2010, accounting for between 1.1% and 1.5% of total electricity use [1]. Many system components in the data center contribute to the overall power consumption, including servers, power, cooling, storage, networking equipment, etc. Nowadays, many network devices have tended to integrate additional functionalities to sleep when not being used and automatically wake up when receiving requests. By shutting down wireless network card of a handheld device when no internet action is being taken place, the battery lifetime can be increased. In this case, the network card is powered only when an incoming call is received. This is known as “wake-on-wireless” [2]. Moreover, the IEEE 802.1X Wake on LAN (WOL) [3] supporting feature allows dormant PCs to be

powered up when the switch receives a specific Ethernet frame, known as the “magic packet” [4].

Following this trend, some power management methods for networking devices have been proposed to reduce network power consumption, can be generally divided into two categories: the sleep mode supporting devices [5, 6] and rate adaptation mechanism supporting devices [7, 8]. Sleeping scheme powers off idle devices or components into sleep states [6] for a pre-estimated duration, and wakes up the sleeping devices or components when new packets arrive. However, this scheme is fragile against burst traffic [8]. In [9] and [10], a framework called ECODANE (Reducing Energy Consumption in Data Center Networks based on Traffic Engineering)¹ was proposed. It focuses on optimizing the power consumption of network components by designing an intelligent network control system that dynamically adapts the set of active network components corresponding to the total traffic going through the data center. The experimental results in [9] and [10] have shown that by disabling unused links (i.e. ports) and switches, an energy saving of 25% to 40% can be achieved. In [11], a Clock Controller (CC) which receives control messages from an OpenFlow controller and adapts the working clock frequency of the switch according to traffic throughput to save energy was designed. Such a framework, however, requires the use of a more flexible and configurable network architecture such as Software-Defined Networking (SDN), in which the OpenFlow is one of

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the technologies widely used. There have been attempts to extend the current commercial switches to support OpenFlow protocols [12] [13] or to build a complete OpenFlow switch for research purposes [14]. However, these switches do not have power aware functionalities including SLEEP modes and WOL. In this paper, we propose methods for intelligently controlling the power consumption of OpenFlow switches used in data centers by adding SLEEP modes and WOL mechanism to the switches. The main contributions of our work are the following:

- We define two new sleep modes: SLEEP PORT mode and SLEEP SWITCH mode.
- We design a new WOL module for NetFPGA based OpenFlow Switches which can wake up Ethernet ports or switch when they are in a sleep mode.

The rest of the paper is organized as follows. Section II defines two new sleep modes for OpenFlow switches. Section III presents the design of the new WOL module for OpenFlow Switches. Section IV describes experimental results. Conclusions are drawn in section V.

II. SLEEP MODES FOR OPENFLOW SWITCHES

In [11] we designed a clock controller module integrated in the core of the NetFPGA based OpenFlow switch which can adjust the working clock frequency of the switch from 125 MHz down to 3.90625 MHz as in Fig.1.

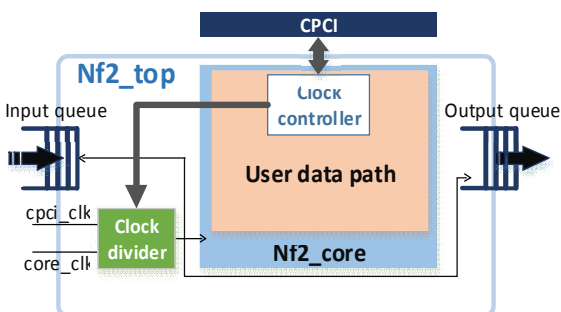


Figure 1. Structure of the frequency divider

We could also change the state of any port of the switch to idle mode by modifying some bits in the control register in the Ethernet control chip [19].

From these results we define two new sleep modes as follows.

- SLEEP PORT mode: This mode is used to turn off one or more Ethernet port when there is no traffic flowing through the ports. In this mode, the switch is running at 125 MHz in order to maintain the operation of other Ethernet ports.
- SLEEP SWITCH mode: This mode is activated only when there is not any traffic going through any Ethernet port. In this case, the switch does not need to process the data flow and can be running at the minimum clock frequency of 3.90625 MHz, while three out of the four Ethernet ports are completely turned off. In this mode, switch still maintains the operation of one Ethernet port at 10 Mbps so that the switch can be waken-up immediately to normal operation by WOL method.

III. DESIGN NEW WOL MODULE FOR OPENLOW SWITCHES

In Section II, we present two sleep modes for OpenFlow switches to save power consumption. In order to wake up a port or the whole switch from a sleep mode, we can send an OpenFlow control message to the switch. However, in many cases, sending OpenFlow control messages to wake up a number of switches in the network at the same time can take a long time. To resolve this problem, we propose to add a new WOL module to OpenFlow Switches with this new function, an Ethernet port or a switch can auto-wake up when they receive a broadcast packet (WOL packet) from other devices in the network.

A. Wake On Lan packet

WOL is hardware and software technology to wake-up sleeping systems by sending one or more special coded network packets to target machines which are equipped and enabled to respond to those packets. This additional functionality allows administrators to perform maintenance on systems

Diagram illustrating the structure of the 64-bit MAC address:

- Header:** 6x FF (6 bits)
- 48-bit MAC address:** 33, 44, 55 (48 bits)
- Repeated 16 times MAC address:** 66, 11, 22, ..., 66 (160 bits)

Figure 2. The standard WOL packet

Figure 1 illustrates the bit fields of the I2C peripheral control register. The register is 16 bits wide, organized as follows:

- Reserved:** Bits B15 through B10 (6 bits).
- Switch mode:** Bits B9 and B8 (2 bits).
- Port mode:** Bits B7 through B0 (8 bits), which are further divided into four 2-bit fields:
 - Port 3:** Bits B7 and B6.
 - Port 2:** Bits B5 and B4.
 - Port 1:** Bits B3 and B2.
 - Port 0:** Bits B1 and B0.

Figure 3. Bit meanings of two extended bytes of WOL packet for OpenFlow Switches

Table 1. states of port 0

$\mathbf{b_1b_0}$	State of port
00	off
01	10 Mbps
10	100 Mbps
11	1 Gbps

b₉b₈	Operating Frequency
00	3.90625 MHz
01	125 MHz

B. Design Wake On Lan function for Openflow Switch

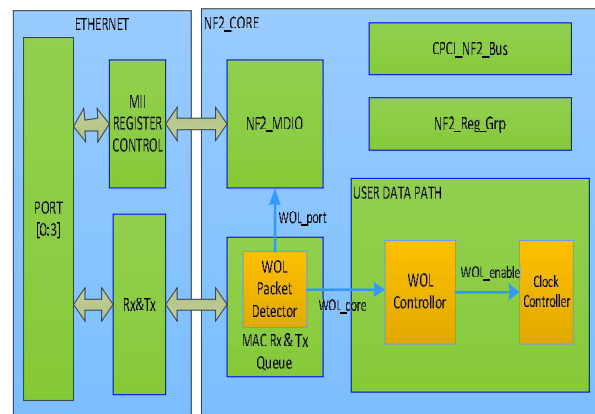


Figure 4. WOL Packet Detector block.

In [15, 16], it is known that to enable WOL function, the network adapter must stay power on even if the PC is shut down. The BIOS must be configured to accept the WOL signal and the operating system/network driver must be configured to keep the network adapter powered on and the motherboard responsive to the WOL signal. Similarly, when a switch operates at the SLEEP SWITCH mode, one Ethernet port still runs at 10 Mbps to listen to a WOL packet. At the MAC RX & TX queue blocks, we build a WOL packet detector block that detects the WOL packet. As shown in Fig.4, the output signals of this block are connected to the NF2_MDIO block that controls the SLEEP PORT mode and to the WOL Controller that controls the Sleep Switch mode.

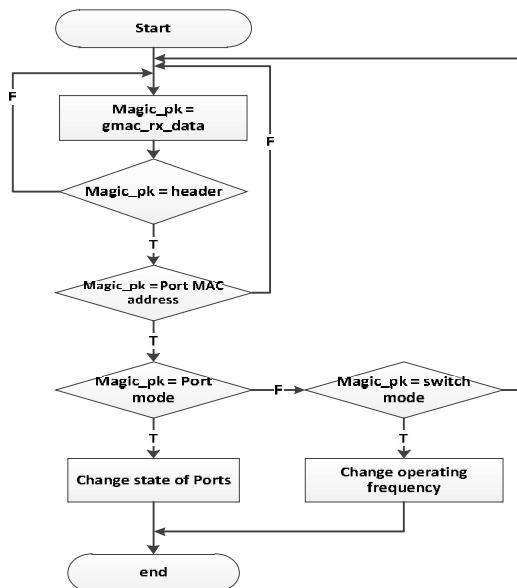


Figure 5. WOL Packet Detector block working principle

When a WOL packet is sent to the switch by other devices on LAN network through the listening Ethernet port, it will be recognized over the bytes header. This packet is compared with the MAC address of the listening port. If it is the same, WOL packet is continuously compared with port mode and switch mode located at the extended bytes defined in part A. WOL Packet Detector block will send WOL_port signal that corresponds to the port. This signal is connected to the NF2_MDIO block that can change the status of the port. We toggle the 11th bit of

the MII register [11] to '1' to turn-on the port. And we use a combination of the 6th bit and the 13th bit to change the bandwidth on each port.

Besides, WOL Packet Detector block also sends WOL_core signal to the WOL Controller block to control the Clock Controller block which is presented in paper [11]. This block will change the operating frequency of the switch to 3.90625 MHz or to 125MHz. The working principle of the WOL Packet Detector is shown in Fig.5.

IV. EXPERIMENTAL RESULTS

C. Power of Switch at two sleep modes

In order to measure saving power consumption at the two sleep modes defined in Section II, we build a hardware test-bed including a NOX Controller, and an OpenFlow Switch based on NetFPGA-1G board as in Fig.6.



Figure 6. Test-bed system for measurement.

The NOX controller version 1.0.0 is implemented on a host PC running Ubuntu version 10.10. OpenFlow switch version 1.0.0.4 based on NetFPGA version 3.0.1 developed by Stanford [17] is used. We also use PC1 and PC2 to generate packets on links. PC1 and PC2 will exchange data at hard load of bandwidth. Oscilloscope and Power Measure Board are used to read ADC value at the test-point 3.3V and 5.0V via PCIEXT-64UB [18] and then display, and calculate the power consumed.

Measurement results of the power consumption of a NetFPGA based OpenFlow switch with two different sleep modes (i.e.: SLEEP PORT mode and SLEEP SWITCH mode) are shown in Table 3.

In paper [11], we measured the total energy consumption of the switch when all four ports operate at a bandwidth of around 1 Gbps and we obtained the result of 11580 mW. This is the largest power consumption of the switch under normal operation. With the proposed sleep modes, the switch can save about 9.8% of the total power consumption when one port is in the SLEEP PORT mode and up to about 60% if the switch is put to the SLEEP SWITCH mode.

Table 3. OpenFlow switch Power consumption at different sleep modes

Mode	Power Consumption of Switch (mW)
Sleep one port	10434
Sleep two ports	9299
Sleep three ports	8203
Sleep switch	4576

D. Test Wake On Lan method for Openflow switch

We also design the other test-bed system to wake up switch when it runs at sleep modes by other (another) PC.(Fig.7)

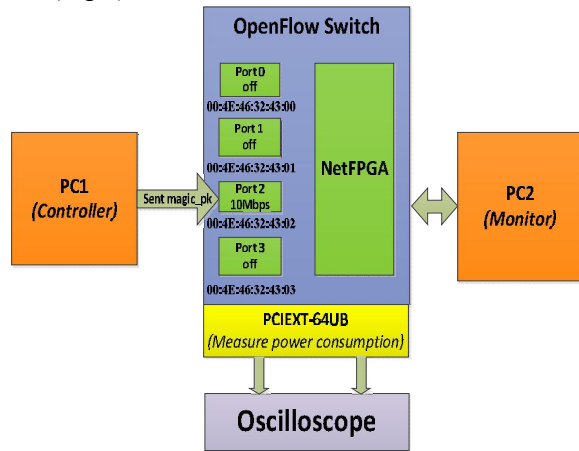


Figure 7. Testbed system for Wake On Lan function

As shown in Fig.7, PC1 plays the role of a controller which has a packet generator to send the WOL packet to the Ethernet port in order to wake up target OpenFlow switch operating in sleep modes. PC2 is used to supervise the working modes of the OpenFlow switch under test.

In our experiment, first, port 0 is turned off, and then a WOL packet is sent to port 2 which is working normally and listening to the WOL packet to wake up port 0. This packet contains the MAC address of the Ethernet port 2 and has the $\{b_0, b_1\}$ bits set to "11". As depicted in Fig.8 after port 2 receives a WOL packet, port 0 is waken up successfully.

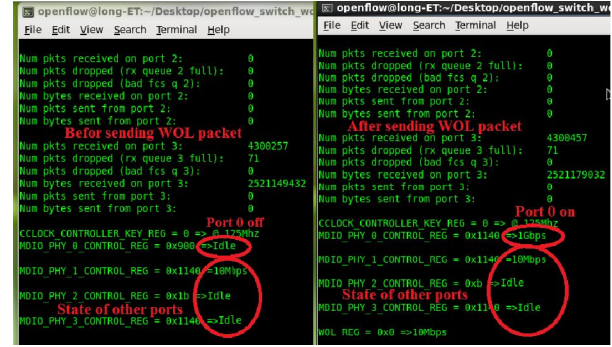


Figure 8. Monitor states of switch when wakes up port 0

In the second stage of the test, the OpenFlow switch is set to work in SLEEP SWITCH mode at which switch runs at frequency of 3.90625 MHz and three ports are turned off, port 2 is running at 10 Mbps to listen the WOL packet. Then PC1 sends the WOL packet to wake the switch up to normal operation. This packet contains the MAC address of port 2 and has extended bytes as shown in Fig.9.

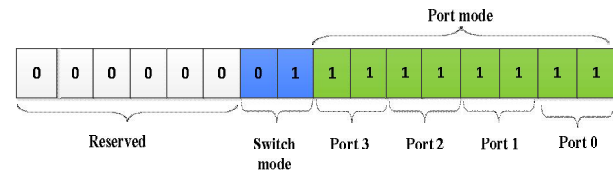


Figure 9. Extended bytes to wake up switch

After port 2 receives the WOL packet, the switch is waken up successfully and operate in normal state. PC2 also captures all monitored states of the switch, as shown in Fig.10.


```

openflow@long-ET:~/Desktop/openflow_switch_wol
File Edit View Search Terminal Help
Num pkts received on port 2: 0
Num pkts dropped (rx queue 2 full): 0
Num pkts dropped (bad fcs q 2): 0
Num bytes received on port 2: 0
Num pkts sent from port 2: 0
Num bytes sent from port 2: 0
Before sending WOL packet
Num pkts received on port 3: 4380461
Num pkts dropped (rx queue 3 full): 71
Num pkts dropped (bad fcs q 3): 0
Num bytes received on port 3: 2521179032
Num pkts sent from port 3: 0
Num bytes sent from port 3: 0
Switch off
CCLOCK_CONTROLLER_KEY_REG = 7 = 0x3306250b
MDIO_PHY_0_CONTROL_REG = 0xdeadbeef
MDIO_PHY_1_CONTROL_REG = 0xdeadbeef =>10Mbps
MDIO_PHY_2_CONTROL_REG = 0xdeadbeef =>Idle
MDIO_PHY_3_CONTROL_REG = 0xdeadbeef =>Idle

openflow@long-ET:~/Desktop/openflow_switch_wol
File Edit View Search Terminal Help
Num pkts received on port 2: 0
Num pkts dropped (rx queue 2 full): 0
Num pkts dropped (bad fcs q 2): 0
Num bytes received on port 2: 0
Num pkts sent from port 2: 0
Num bytes sent from port 2: 0
After sending WOL packet
Num pkts received on port 3: 4380457
Num pkts dropped (rx queue 3 full): 71
Num pkts dropped (bad fcs q 3): 0
Num bytes received on port 3: 2521179032
Num pkts sent from port 3: 0
Num bytes sent from port 3: 0
Switch on
CCLOCK_CONTROLLER_KEY_REG = 0 = 0x1290b2
MDIO_PHY_0_CONTROL_REG = 0x1140 =>10Mbps
MDIO_PHY_1_CONTROL_REG = 0x1140 =>10Mbps
MDIO_PHY_2_CONTROL_REG = 0x1140 =>10Mbps
MDIO_PHY_3_CONTROL_REG = 0x1140 =>10Mbps

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Figure 10. Monitor the waking up of the switch from the SLEEP SWITCH mode

E. Proposed solution in the Future

In the future, our group will implement this solution to NetFPGA-10G [20]. The 10G NetFPGA platform provides 4 x 10 Gigabit Ethernet SFP+ interfaces which are operated by AEL2005 PHYs, and two Samtec expansion connectors which are operated by 20 GTX dual transceivers. The PHYs are connected to a Xilinx Virtex-5 TX240T and communicate to XGMAC cores on the FPGA in full duplex mode.

Because this version of OpenFlow Switch has bandwidth 10Gig/1port that consumes power higher than OpenFlow Switch 1Gig, we strongly believe that our method will save a large amount of energy for OpenFlow Switch.



Figure 11. NetFPGA-10G

II. CONCLUSIONS AND FUTURE WORKS

In this paper, we have defined and implemented two sleep modes for OpenFlow Switches to reduce power consumption. We have also implemented WOL method to wake up an NetFPGA based OpenFlow Switch from sleep modes to normal state. We also built the test-bed system and precisely measured the energy of the whole switch saving of about 9.8% power consumption per port, and up to

about 60% of total power consumption of the switch with SLEEP SWITCH mode.

In the future, we will implement this method to Openflow Switch 10 Gig and use in the design of power aware commercial OpenFlow Switches.

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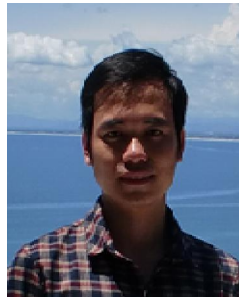
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